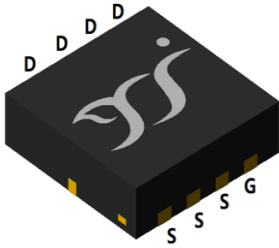
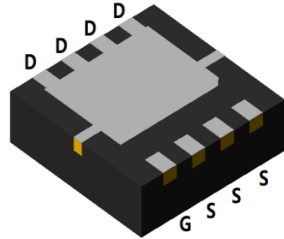


N-Channel Enhancement Mode Field Effect Transistor

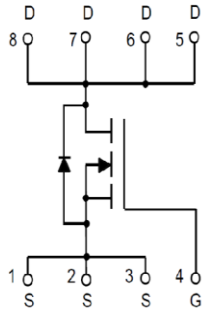


Top View



Bottom View

DFN3333-8L



Product Summary

- V_{DS} 60V
- I_D (Silicon limited) 62A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) < 7.5 mohm
- $R_{DS(ON)}$ (at $V_{GS}=4.5V$) < 10 mohm
- 100% EAS Tested

General Description

- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 3
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- DC-DC Converters
- Power management functions
- Industrial and Motor Drive application

■ Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	60	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current (Silicon limited)	$T_A=25^\circ C$	I_D	12	A
	$T_A=100^\circ C$		7.5	
	$T_C=25^\circ C$		62	
	$T_C=100^\circ C$		39	
Pulsed Drain Current ^A		I_{DM}	186	A
Avalanche energy ^B		E_{AS}	162	mJ
Total Power Dissipation ^C	$T_A=25^\circ C$	P_D	2.2	W
	$T_A=100^\circ C$		0.9	
	$T_C=25^\circ C$		45	
	$T_C=100^\circ C$		18	
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	$^\circ C$

■ Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient ^D	$t \leq 10S$	$R_{\theta JA}$	18	22	$^\circ C/W$
Thermal Resistance Junction-to-Ambient ^D	Steady-State		45	55	
Thermal Resistance Junction-to-Case	Steady-State		$R_{\theta JC}$	2.3	

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJQ62G06A	F1	Q62G06	5000	10000	100000	13" reel



YJQ62G06A

■ Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250μA	60			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =60V, V _{GS} =0V	T _J =25°C		1	μA
			T _J =55°C		5	
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA	1.2	1.7	2.5	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} = 10V, I _D =20A		5.8	7.5	mΩ
		V _{GS} = 4.5V, I _D =10A		7.3	10	
Diode Forward Voltage	V _{SD}	I _S =20A, V _{GS} =0V		0.85	1.3	V
Maximum Body-Diode Continuous Current	I _S				62	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =35V, V _{GS} =0V, f=1MHZ		2000		pF
Output Capacitance	C _{oss}			390		
Reverse Transfer Capacitance	C _{rss}			13		
Gate Resistance	R _g	f=1MHZ, Open drain		1.6		Ω
Switching Parameters						
Total Gate Charge	Q _g (10V)	V _{DS} =30V, I _D =20A		34		nC
Total Gate Charge	Q _g (4.5V)			15.8		
Gate-Source Charge	Q _{gs}			7.8		
Gate-Drain Charge	Q _{gd}			5.2		
Reverse Recovery Charge	Q _{rr}	I _F =20A, di/dt=200A/us		36		
Reverse Recovery Time	t _{rr}			27		
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DD} =30V, I _D =12A R _{GEN} =3Ω		10		ns
Turn-on Rise Time	t _r			36		
Turn-off Delay Time	t _{D(off)}			30		
Turn-off fall Time	t _f			57		

A. Repetitive rating; pulse width limited by max. junction temperature.

B. V_{DD}=50V, R_G=25Ω, L=1mH, I_{AS}=18A,.

C. Pd is based on max. junction temperature, using junction-case thermal resistance.

D. The value of R_{θJA} is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The Power dissipation P_{DSM} is based on R_{θJA} t_s ≤ 10s and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.



■ Typical Performance Characteristics

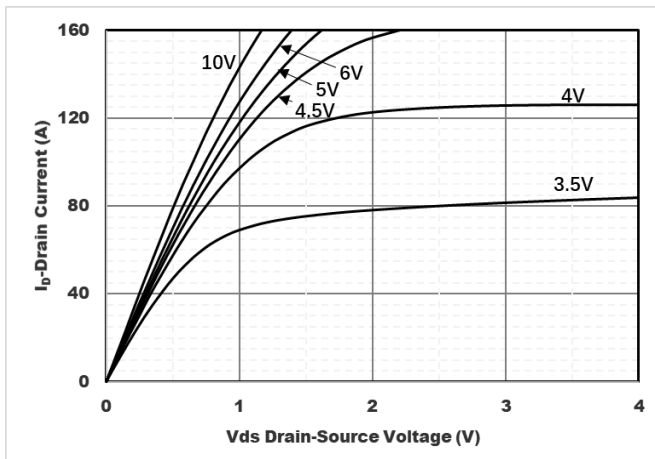


Figure1. Output Characteristics

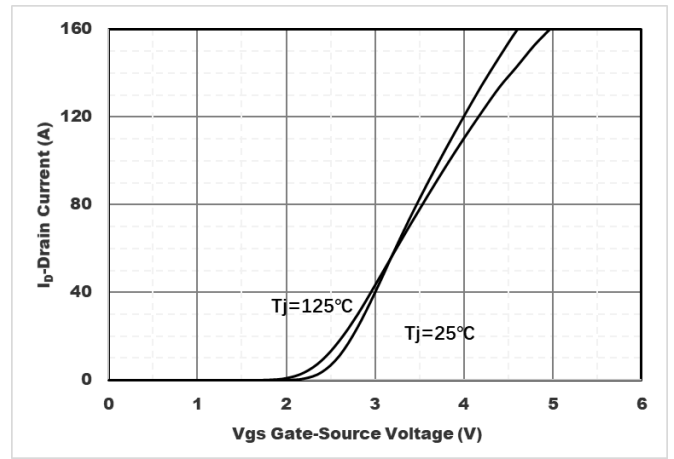


Figure2. Transfer Characteristics

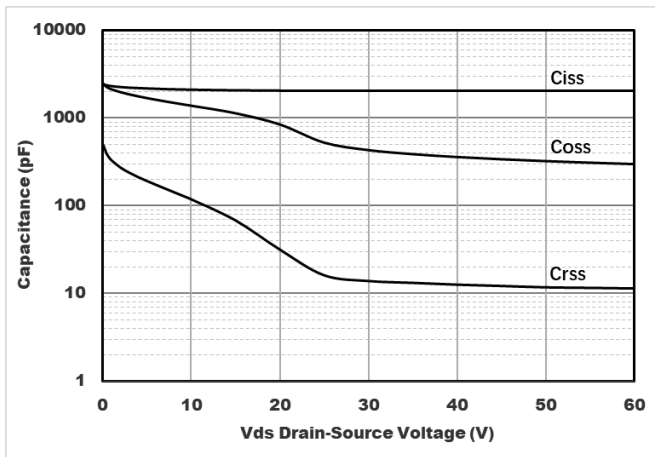


Figure3. Capacitance Characteristics

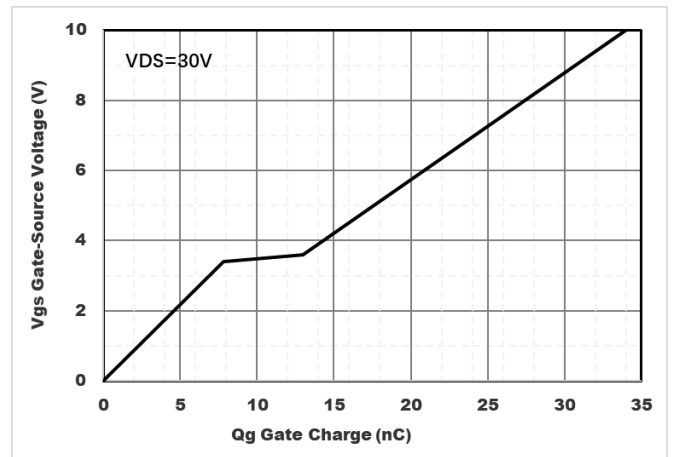


Figure4. Gate Charge

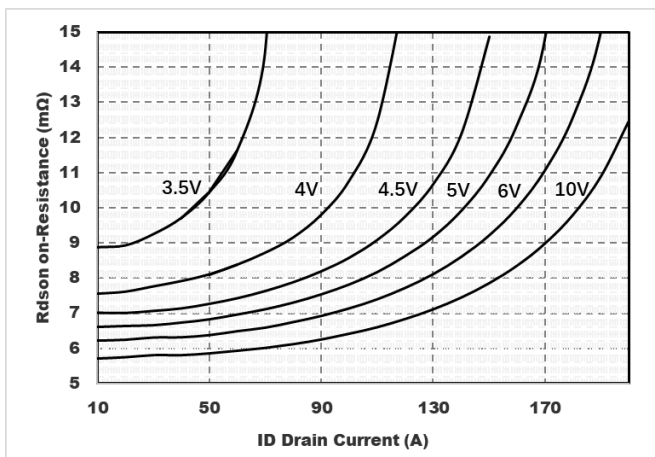


Figure5. Drain-Source on Resistance

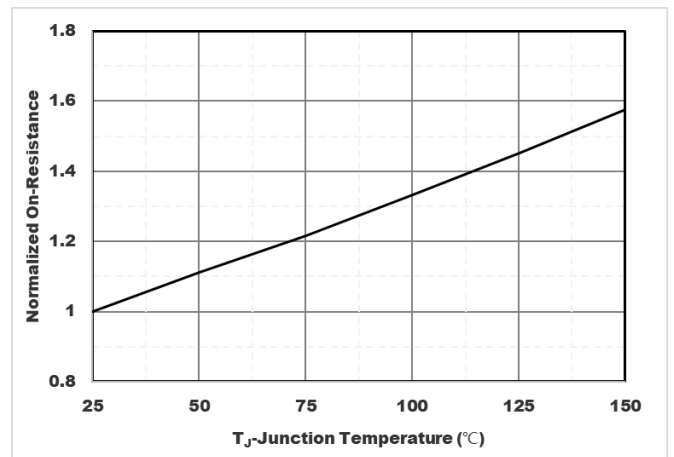


Figure6. Normalized On-Resistance



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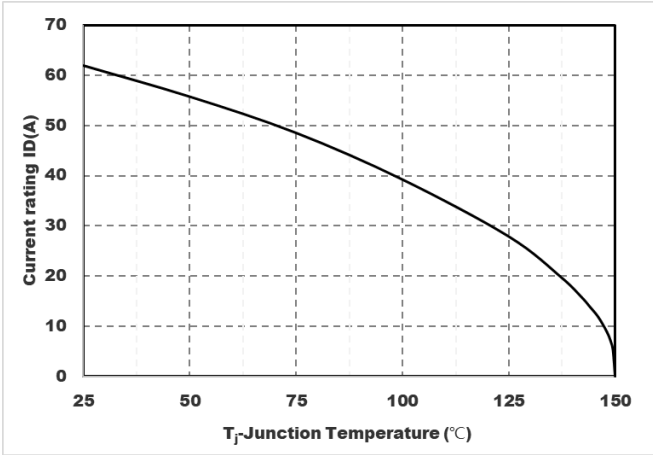


Figure7. Drain current

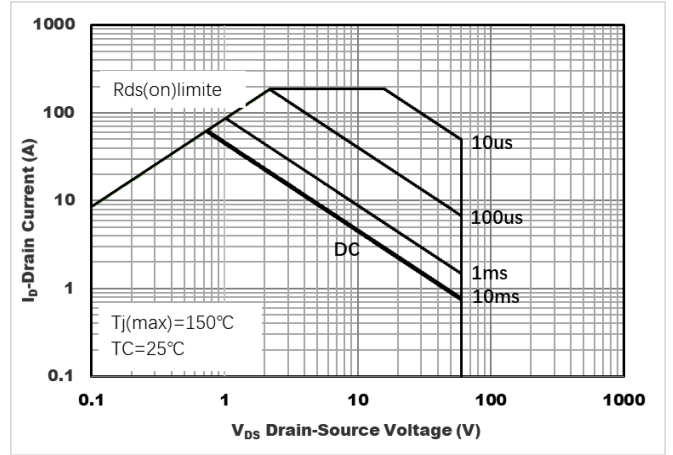


Figure8. Safe Operation Area

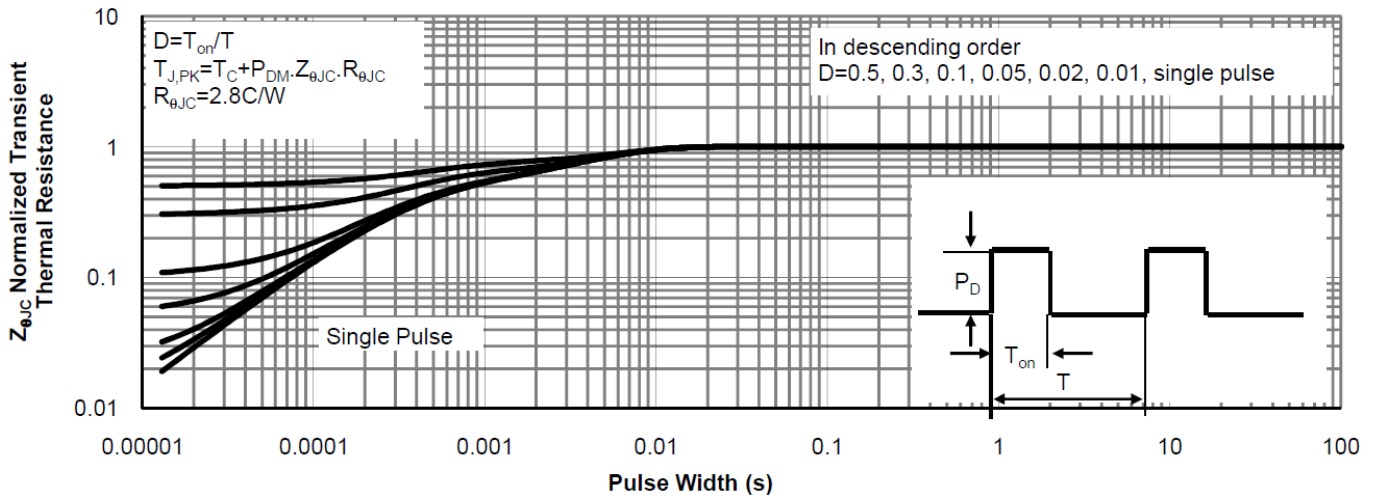
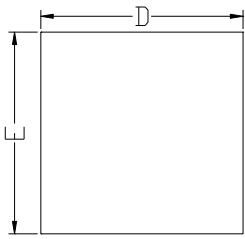


Figure8. Normalized Maximum Transient Thermal Impedance

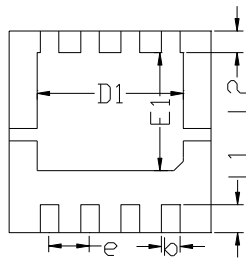


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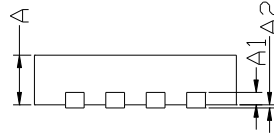
DFN3333-8L Package information



Top View
正面视图

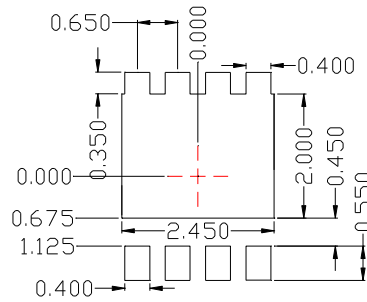


Bottom View
背面视图



Side View
侧面视图

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	3.15	3.25	3.35
E	3.15	3.25	3.35
A	0.70	0.80	0.90
A1	0.20 BSC		
A2			0.10
D1	2.20	2.35	2.50
E1	1.80	1.90	2.00
L1	0.35	0.45	0.55
L2	0.35 BSC		
k	0.20	0.30	0.40
e	0.65 BSC		



Suggested Solder Pad Layout
Top View

Note:

1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.10\text{mm}$.
3. The pad layout is for reference purposes only.



YJQ62G06A

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