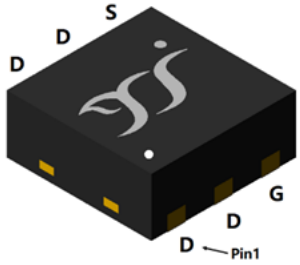
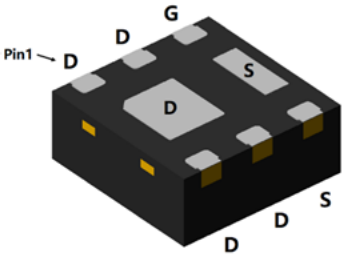
N-Channel Enhancement Mode Field Effect Transistor

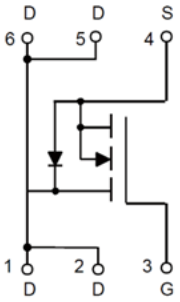


Top View



Bottom View

DFN2020-6L



Product Summary

- V_{DS} 30V
- I_D 13A
- $R_{DS(ON)}$(at V_{GS}=10V) ＜12 mohm
- $R_{DS(ON)}$(at V_{GS}=4.5V) ＜15 mohm

General Description

- Trench Power LV MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- High current load applications
- Load switching
- Hard switched and high frequency circuits
- Uninterruptible power supply

■ Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	30	V
Gate-source Voltage		V_{GS}	±20	V
Drain Current	T_A=25℃	I_D	13	A
	T_A=100℃		8.0	
Pulsed Drain Current [A]		I_{DM}	55	A
Total Power Dissipation	T_A=25℃	P_D	2.9	W
	T_A=100℃		1.2	W
Thermal Resistance Junction-to-Ambient [B]		$R_{\theta JA}$	43	℃/ W
Junction and Storage Temperature Range		T_J ,T_{STG}	-55～+150	℃

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJQ13N03A	F1	Q13N03	3000	30000	120000	7” reel

■ Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Static Parameter							
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA		30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=30V,V_{GS}=0V	T_J=25℃			1	μA
			T_J=55℃			5	
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V				±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA		1.0	1.5	2.5	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}= 10V, I_D=8A			7	12	mΩ
		V_{GS}= 4.5V, I_D=5A			11	15	
Diode Forward Voltage	V_{SD}	I_S=13A,V_{GS}=0V				1.2	V
Maximum Body-Diode Continuous Current	I_S					13	A
Dynamic Parameters							
Input Capacitance	C_{iss}	V_{DS}=15V,V_{GS}=0V,f=1MHZ			1015		pF
Output Capacitance	C_{oss}				201		
Reverse Transfer Capacitance	C_{rss}				164		
Switching Parameters							
Total Gate Charge	Q_g	V_{GS}=10V,V_{DS}=20V,I_D=20A			23.6		nC
Gate-Source Charge	Q_{gs}				3.8		
Gate-Drain Charge	Q_{gd}				7		
Reverse Recovery Charge	Q_{rr}	I_F=15A, di/dt=100A/us			0.2		
Reverse Recovery Time	t_{rr}				5		ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V,V_{DD}=20V, I_D=2A, R_{GEN}=3Ω			7		
Turn-on Rise Time	t_r				20		
Turn-off Delay Time	$t_{D(off)}$				24		
Turn-off fall Time	t_f				24		

A. Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.

B. $R_{\theta JA}$ is the sum of the junction-to-Case and Case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

■ Typical Performance Characteristics

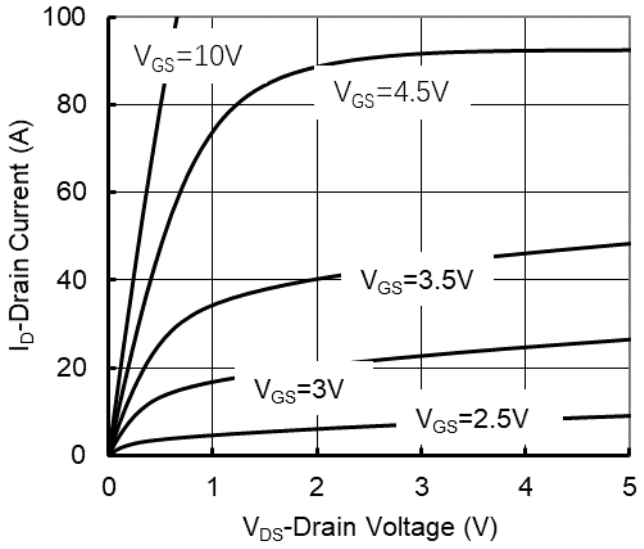


Figure1. Output Characteristics

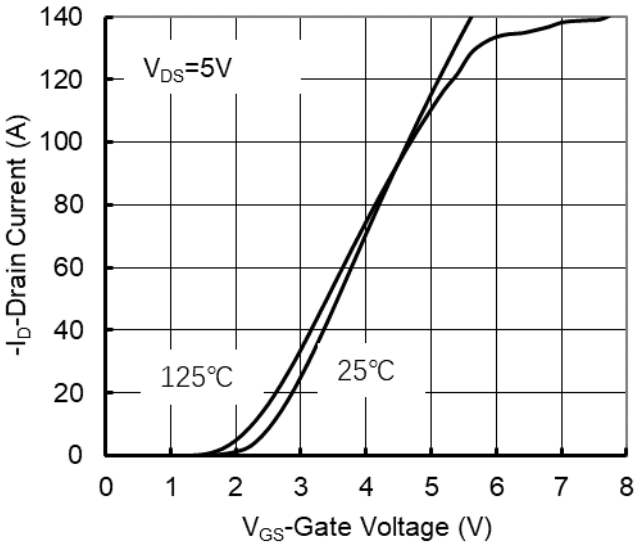


Figure2. Transfer Characteristics

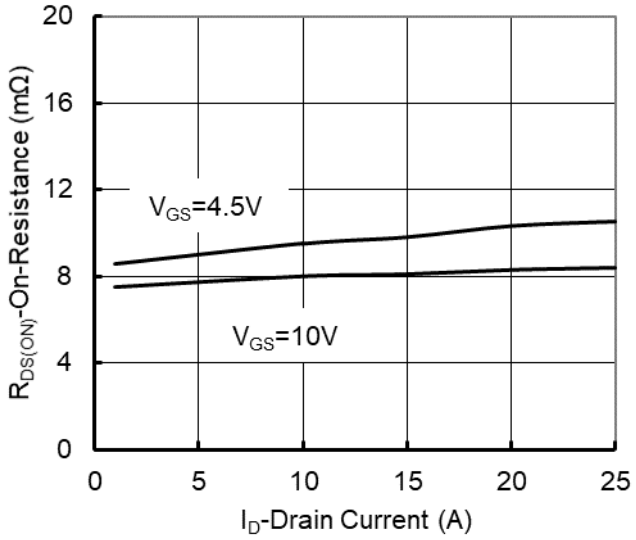


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

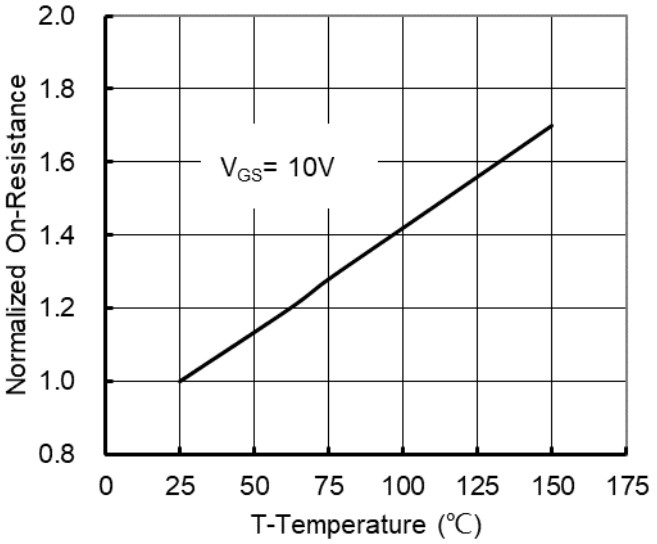


Figure 4: On-Resistance vs. Junction Temperature

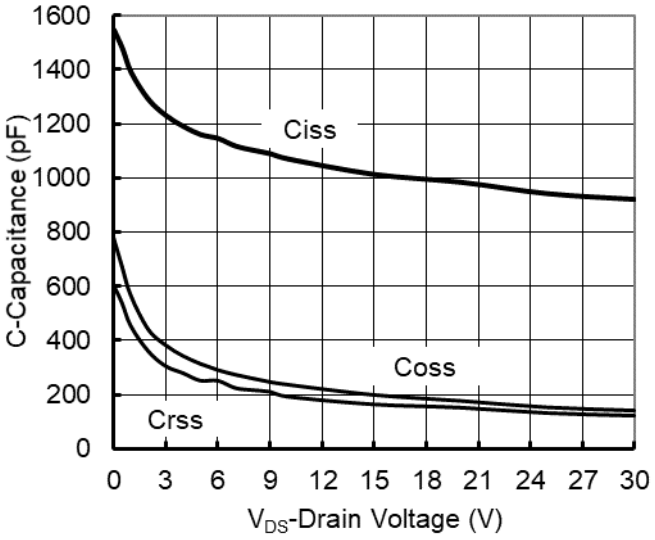


Figure5. Capacitance Characteristics

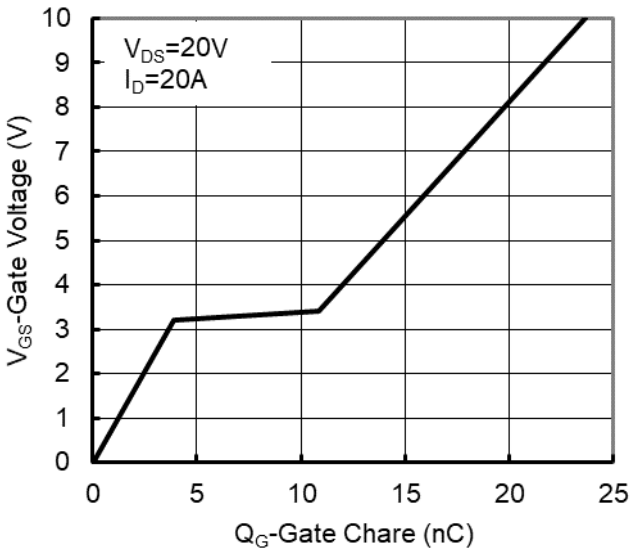


Figure6. Gate Charge

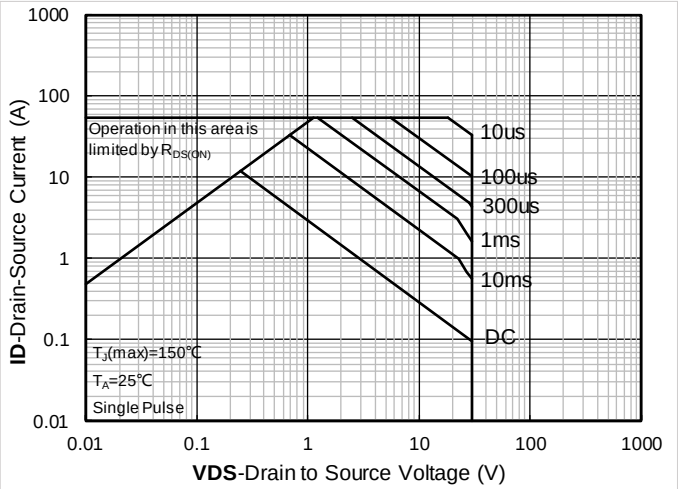


Figure7. Safe Operation Area

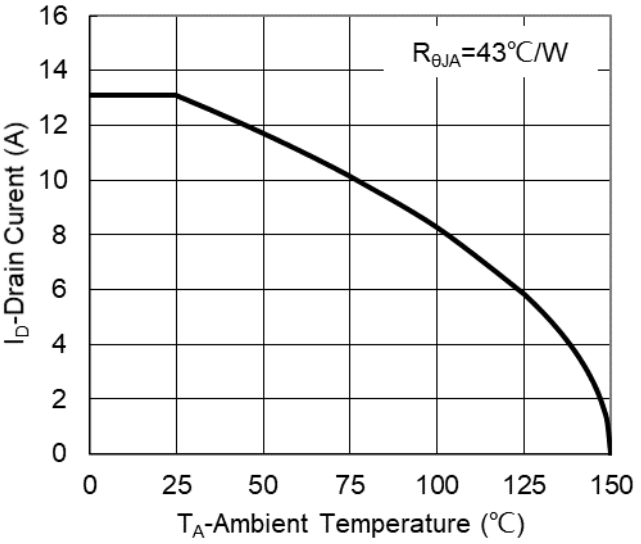


Figure8. Maximum Continuous Drain Current vs Ambient Temperature

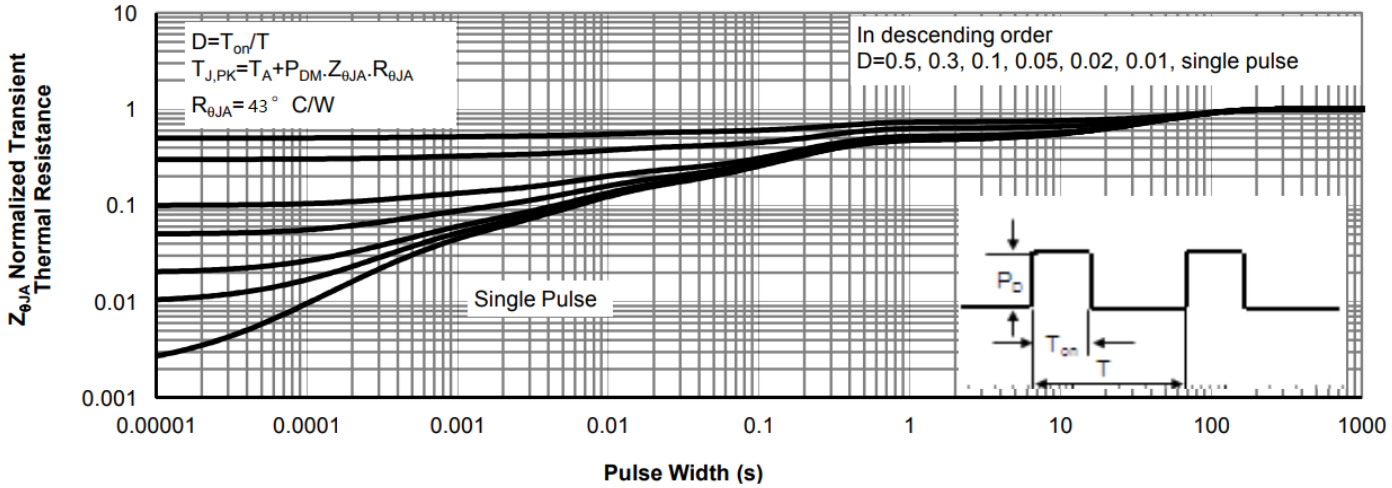
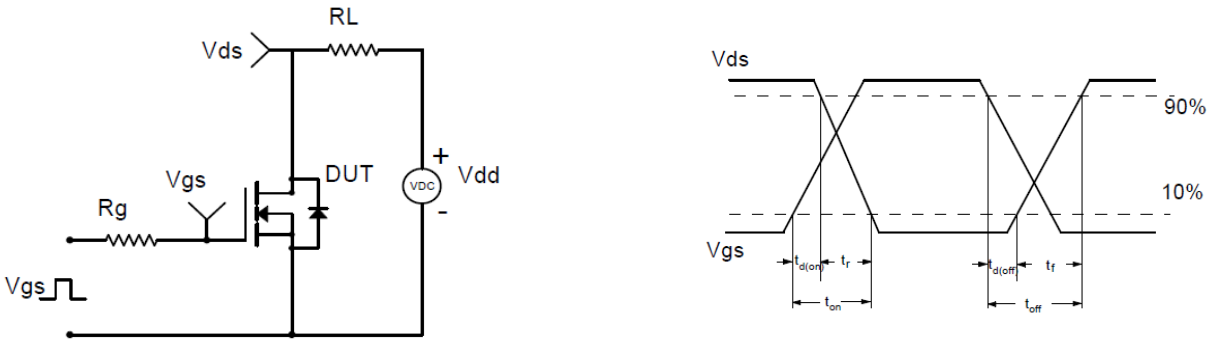
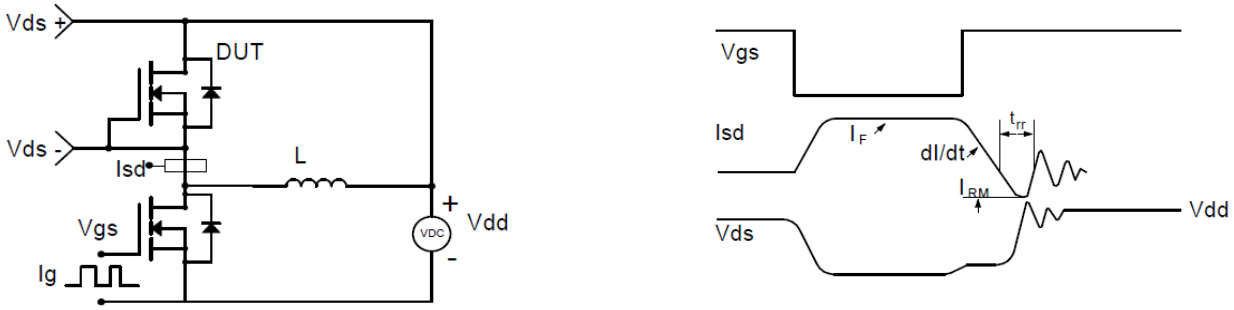


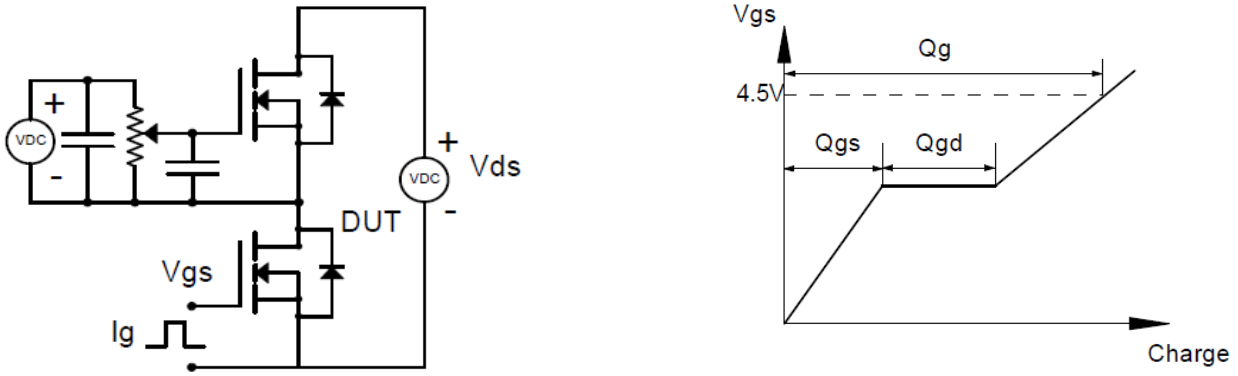
Figure9.Normalized Maximum Transient Thermal Impedance



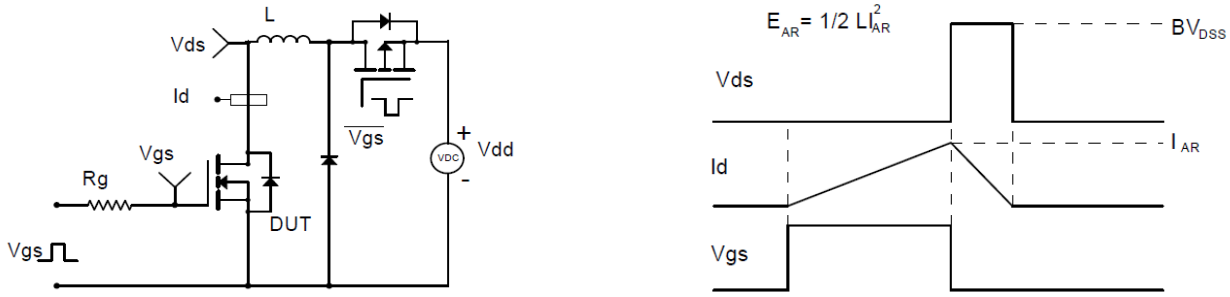
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

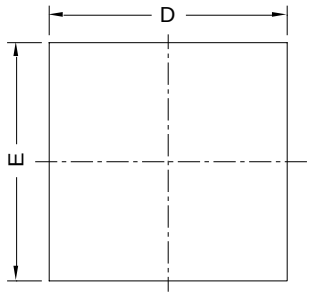


Gate Charge Test Circuit & Waveform

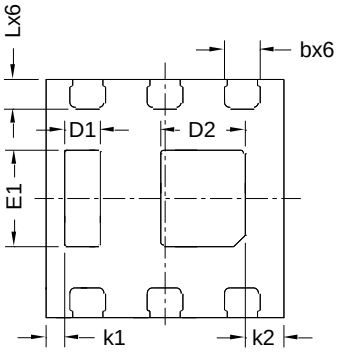


Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

■ DFN2020-6L-E-0.80MM Package information

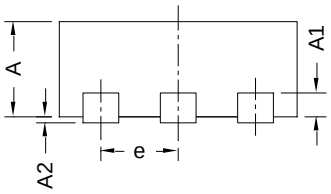


Top View
正面视图

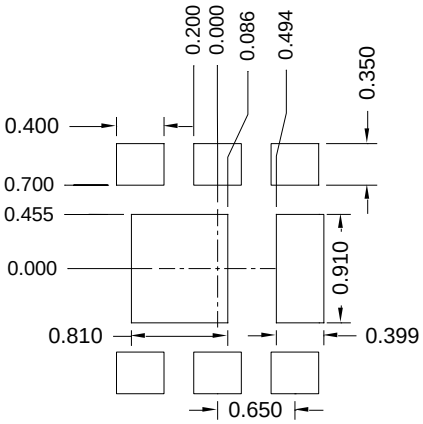


Bottom View
背面视图

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	1.90	2.00	2.10
E	1.90	2.00	2.10
A	0.70	0.80	0.90
A1		0.20 BSC	
A2			0.10
D1	0.20	0.30	0.40
D2	0.61	0.71	0.81
E1	0.71	0.81	0.91
L	0.15	0.25	0.35
b	0.20	0.30	0.40
e		0.65 BSC	
k1		0.156 BSC	
k2		0.326 BSC	



Side View
侧面视图



Suggested Solder Pad Layout
Top View

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.10mm.
3.The pad layout is for reference purposes only.

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