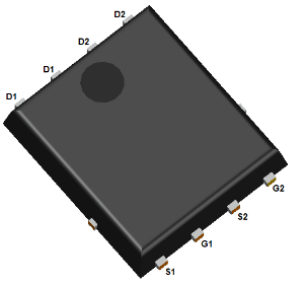
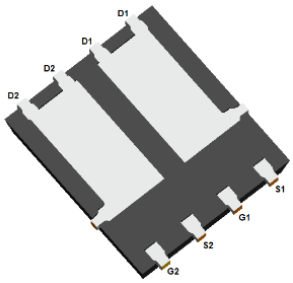
N-Channel Enhancement Mode Field Effect Transistor

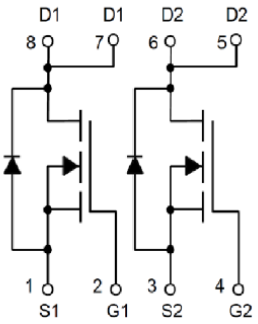


Top View



Bottom View

PDFN5060-8L



Product Summary

NMOS(Die1/Die2)

- V_{DS} 100V
- I_D 20A
- $R_{DS(ON)}$(at V_{GS}=10V) ＜22 mohm
- $R_{DS(ON)}$(at V_{GS}=4.5V) ＜27 mohm

General Description

- Split gate trench MOSFET technology
- High density cell design for low $R_{DS(ON)}$
- High Speed switching
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free
- Part no. with suffix “Q” means AEC-Q101 qualified

Applications

- DC-DC Converters
- Power management functions
- Industrial and Motor Drive application
- 12V, 24V and 48V Automotive systems

■ Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter		Symbol	N-Die1/Die2	Unit
Drain-source Voltage		V_{DS}	100	V
Gate-source Voltage		V_{GS}	±20	V
Drain Current	T_C=25℃	I_D	20	A
	T_C=100℃		13	
	T_A=25℃		7	
	T_A=100℃		4.5	
Pulsed Drain Current [A]		I_{DM}	80	A
Avalanche energy [B]		E_{AS}	81	mJ
Total Power Dissipation[C]	T_C=25℃	P_D	50	W
	T_C=100℃		20	
	T_A=25℃		2.5	
	T_A=100℃		1	
Junction and Storage Temperature Range		T_J ,T_{STG}	-55~+150	℃

■Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient [D]	Steady-State	$R_{\theta JA}$	40	50	℃/W
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	2	2.5	

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJGD20G10BQ	F1	YJGD20G10B	5000	10000	100000	13“ reel

■ NMOS(Die1/Die2) Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA	100			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100V,V_{GS}=0V			1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	1.0	1.8	2.5	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}= 10V, I_D=20A		16	22	mΩ
		V_{GS}= 4.5V, I_D=10A		18	27	
Diode Forward Voltage	V_{SD}	I_S=20A,V_{GS}=0V		0.9	1.3	V
Gate Resistance	R_g	f=1MHz		1.5		Ω
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=25V,V_{GS}=0V,f=1MHZ		1240		pF
Output Capacitance	C_{oss}			740		
Reverse Transfer Capacitance	C_{rss}			25		
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V,V_{DS}=50V,I_D=20A		17		nC
Gate-Source Charge	Q_{gs}			6		
Gate-Drain Charge	Q_{gd}			3		
Reverse Recovery Chrage	Q_{rr}	I_F=20A, di/dt=100A/us		42		
Reverse Recovery Time	t_{rr}			40		ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V,V_{DD}=50V,I_D=20A R_{GEN}=3.0Ω		40		
Turn-on Rise Time	t_r			12		
Turn-off Delay Time	$t_{D(off)}$			55		
Turn-off fall Time	t_f			16		

A. Repetitive rating; pulse width limited by max. junction temperature.
B. V_{DD}=50V, R_G=25Ω, L=2mH, I_{AS}=9A.
C. Pd is based on max. junction temperature, using junction-case thermal resistance.
D. The value of RθJA is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with TA =25° C. The Power dissipation PDSM is based on RθJA t≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.

■ NMOS(Die1/Die2) Typical Performance Characteristics

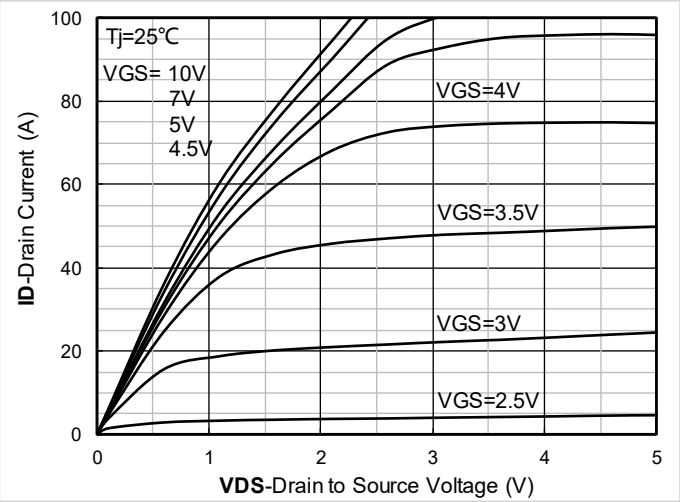


Figure1. Output Characteristics

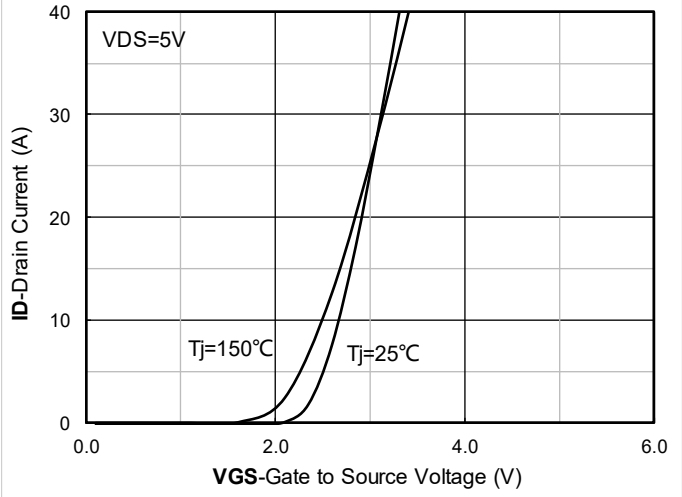


Figure2. Transfer Characteristics

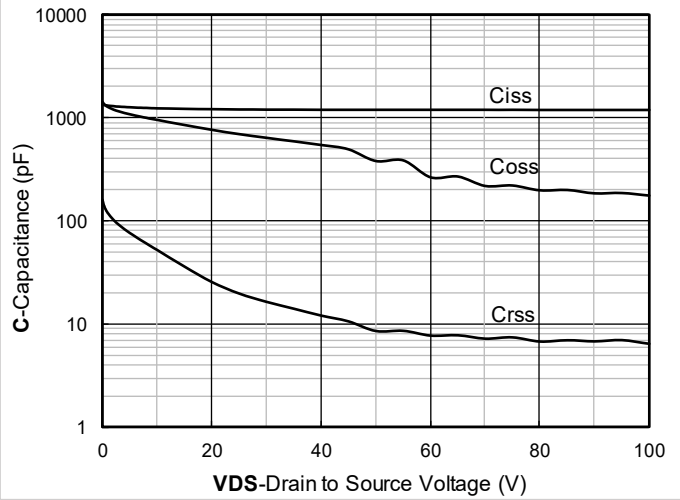


Figure3. Capacitance Characteristics

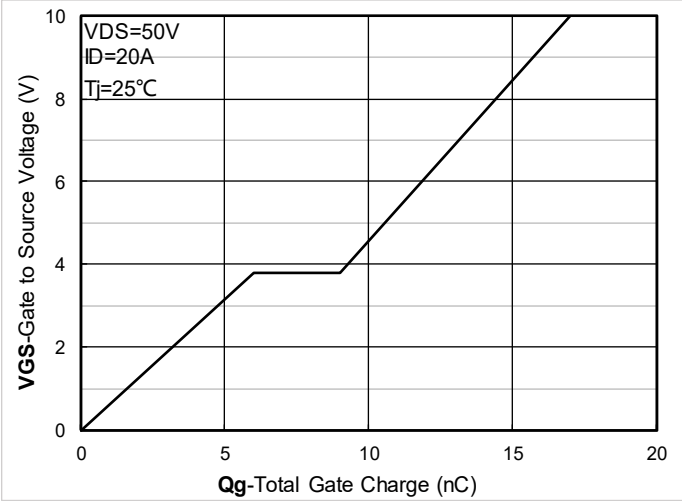


Figure4. Gate Charge

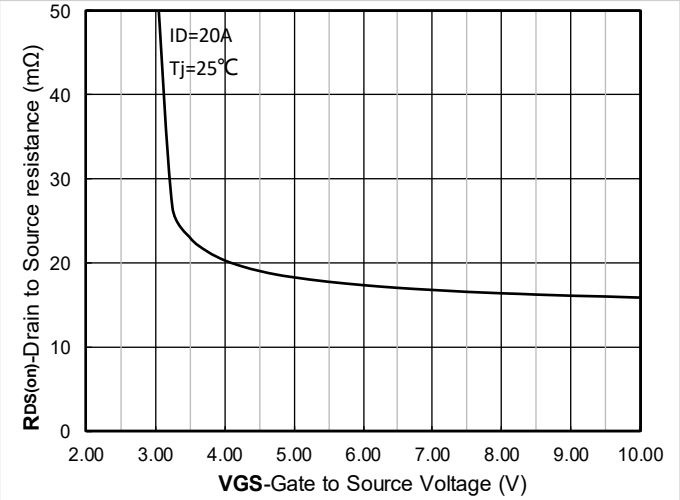


Figure5. On-Resistance vs. Gate to Source Voltage

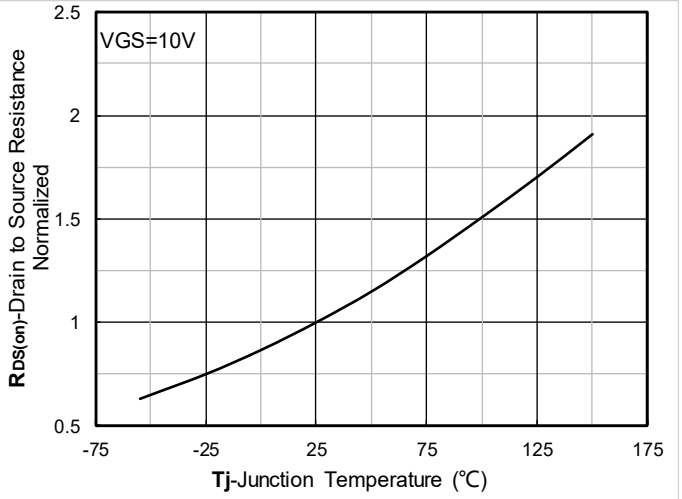


Figure6. Normalized On-Resistance

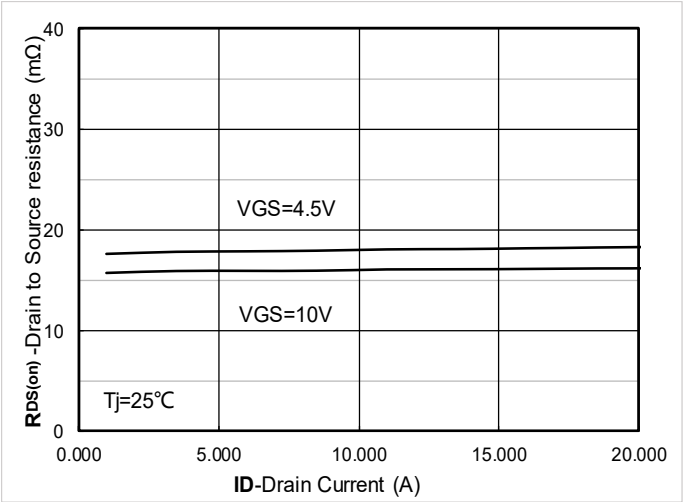


Figure 7. $R_{DS(on)}$ VS Drain Current

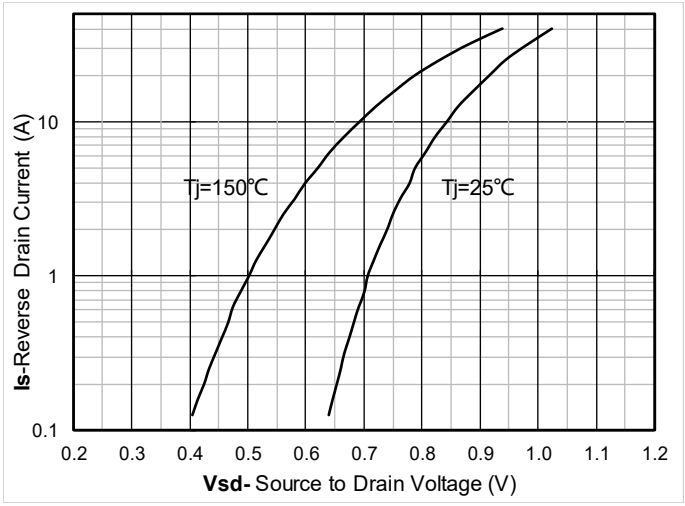


Figure 8. Forward characteristics of reverse diode

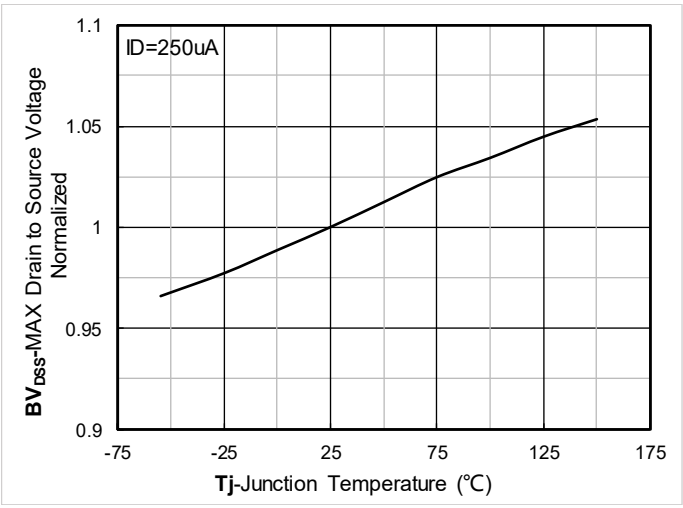


Figure 9. Normalized breakdown voltage

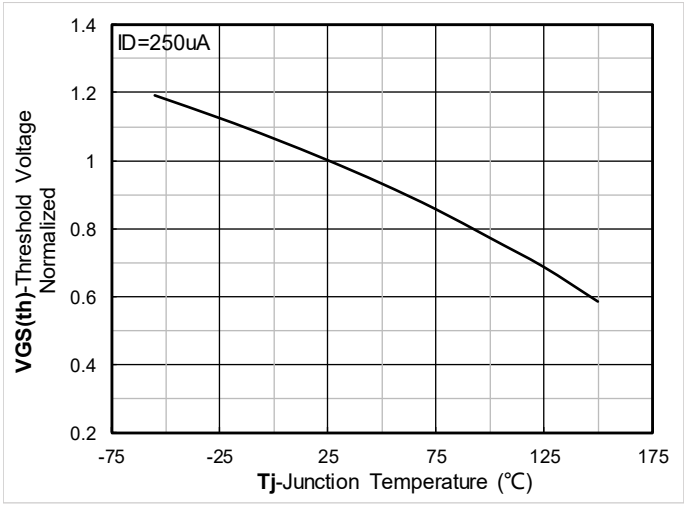


Figure 10. Normalized Threshold voltage

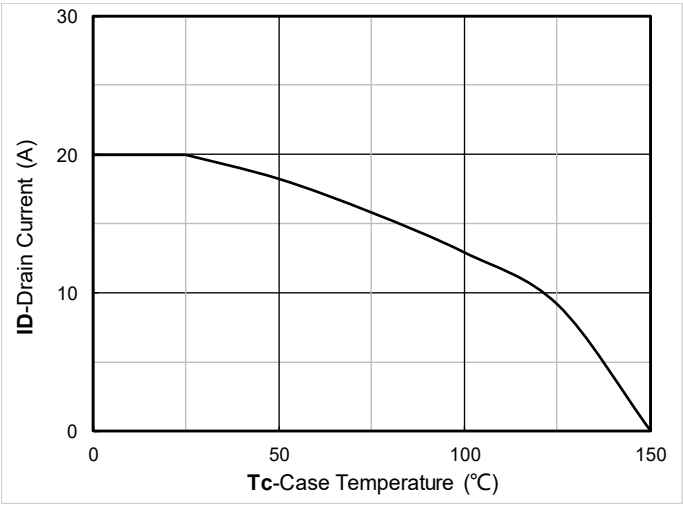


Figure 11. Current dissipation

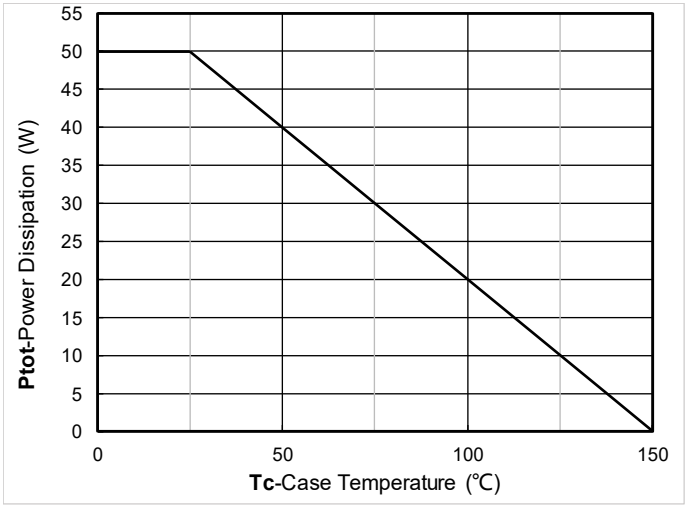


Figure 12. Power dissipation

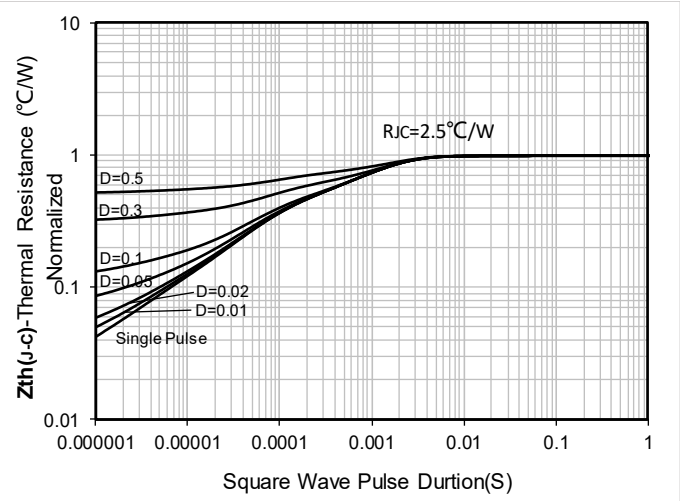


Figure 13. Maximum Transient Thermal Impedance

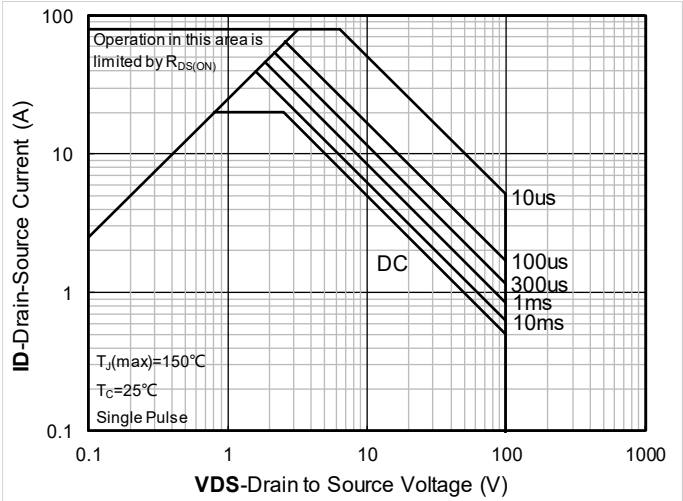
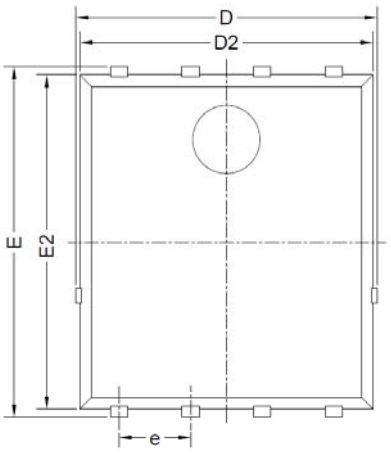
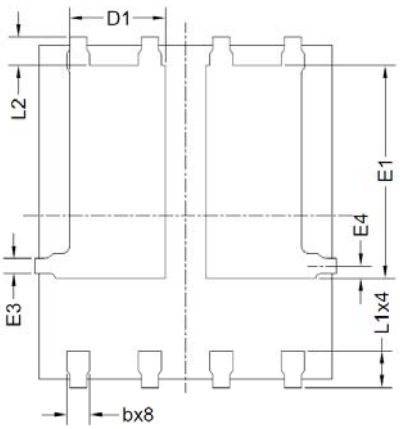


Figure 14. Safe Operation Area

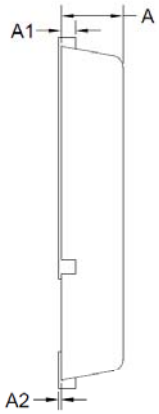
■ PDFN5060-8L Package information



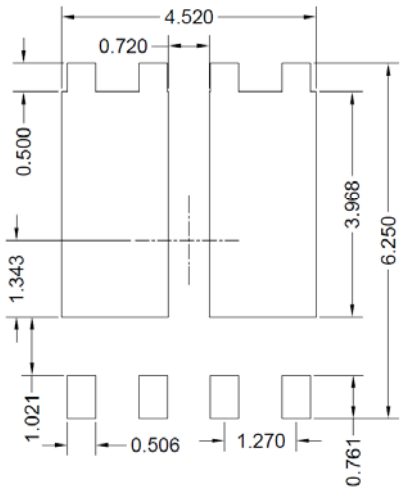
Top View
正面视图



Bottom View
背面视图



Side View
侧面视图



Suggested Solder Pad Layout
Top View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1		0.254 BSC	
A2			0.10
D1	1.50	1.70	1.90
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
E3		0.254REF	
E4		0.21REF	
L1	0.56	0.66	0.76
L2		0.50 BSC	
b	0.31	0.41	0.51
e		1.27 BSC	

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.10mm.
3.The pad layout is for reference purposes only.

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